The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a first transistor;

~~a second transistor~~ a plurality of inverters;

~~a third transistor;~~

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit for ~~applying~~ generating a third potential which is different from the first potential and the second potential,

wherein each of the plurality of inverters comprising:

a second transistor; and

a third transistor,

wherein each of the plurality of inverters is connected to the first power source,

wherein one of a source and a drain of the first transistor is connected to the [[first]] second power source,

wherein the other of the source and the drain of the first transistor is connected to ~~one of a source and a drain of the second transistor~~ each of the plurality of inverters,

~~wherein the other of the source and the drain of the second transistor is connected to one of a source and a drain of the third transistor,~~

~~wherein the other of the source and the drain of the third transistor is connected to the second power source,~~

wherein a gate of the [[third]] first transistor is connected to the circuit,

wherein a first signal is inputted to gates of the [[first]] second transistor and the ~~second~~ third transistor of each of the plurality of the inverters,

wherein a second signal is outputted from ~~the other~~ one of [[the]] a source and [[the]] a drain of the [[first]] second transistor and [[the]] one of [[the]] a source and [[the]] a drain of the ~~second~~ third transistor of each of the plurality of the inverters, and

wherein the first potential is higher than the second potential.

~~wherein the circuit includes multiple resistors connected in series,~~

~~wherein an end of one of the multiple resistors is connected to the first power source,~~

~~wherein an end of another one of the multiple resistors is connected to the second power source, and~~

~~wherein the third potential is outputted from a connecting node of two resistors that are selected from the multiple resistors.~~

2. (Currently Amended) The semiconductor device according to claim 1, ~~wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is a p-channel transistor.~~

wherein the circuit includes multiple resistors connected in series,

wherein an end of the multiple resistors is connected to the first power source,

wherein an end of another one of the multiple resistors is connected to the second power source, and

wherein the third potential is outputted from a connecting node of two resistors that are selected from the multiple resistors.

3. (Currently Amended) A semiconductor device comprising:

a first transistor;

~~a second transistor~~ a plurality of inverters;

~~a third transistor~~;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit for generating a third potential which is different from the first potential and the second potential,

wherein each of the plurality of inverters comprising:

a second transistor; and

a third transistor,

wherein one of a source and a drain of the [[third]] first transistor is connected to the first power source,

wherein the other of the source and the drain of the [[third]] first transistor is connected to ~~one of a source and a drain of the first transistor~~ each of the plurality of inverters,

wherein each of the plurality of inverters is connected to the second power source,

~~wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor,~~

~~wherein the other of the source and the drain of the second transistor is connected to the second power source,~~

wherein a gate of the [[third]] first transistor is connected to the circuit,

wherein a first signal is inputted to gates of the [[first]] second transistor and the ~~second~~ third transistor of each of the plurality of the inverters,

wherein a second signal is outputted from ~~the other~~ one of [[the]] a source and [[the]] a drain of the [[first]] second transistor and [[the]] one of [[the]] a source and [[the]] a drain of the ~~second~~ third transistor of each of the plurality of the inverters, and

wherein the first potential is higher than the second potential.

~~wherein the circuit includes multiple resistors connected in series,~~

~~wherein an end of one of the multiple resistors is connected to the first power source,~~

~~wherein an end of another one of the multiple resistors is connected to the second power source, and~~

~~wherein the third potential is outputted from a connecting node of two resistors that are selected from the multiple resistors.~~

4. (Currently Amended) The semiconductor device according to claim 3, ~~wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is an n-channel transistor.~~

wherein the circuit includes multiple resistors connected in series,

wherein an end of the multiple resistors is connected to the first power source,

wherein an end of another one of the multiple resistors is connected to the second power source, and

wherein the third potential is outputted from a connecting node of two resistors that are selected from the multiple resistors.

5.-6. (Canceled)

7. (Withdrawn) A semiconductor device comprising:

a first transistor;

a second transistor;

a third transistor;

a fourth transistor;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit for generating a third potential which is different from the first potential and the second potential;

wherein one of a source and a drain of the first transistor and one of a source and a drain of the third transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to the second power source;

wherein a gate of the second transistor is connected to the other of the source and the drain of the third transistor and to one of a source and a drain of the fourth transistor;

wherein the other of the source and the drain of the fourth transistor is connected to the circuit;

wherein a first signal is inputted to gates of the first transistor, the third transistor and the fourth transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

8. (Withdrawn) The semiconductor device according to claim 7, wherein the first transistor is a p-channel transistor, the second transistor is a p-channel transistor, the third transistor is a p-channel transistor, and the fourth transistor is an n-channel transistor.

9. (Withdrawn) A semiconductor device comprising:

a first transistor;

a second transistor;

a third transistor;

a fourth transistor;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit for generating a third potential which is different from the first potential and the second potential;

wherein one of a source and a drain of the first transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor and one of a source and a drain of the third transistor is connected to the second power source;

wherein a gate of the first transistor is connected to the other of the source and the drain of the third transistor and to one of a source and a drain of the fourth transistor;

wherein the other of the source and the drain of the fourth transistor is connected to the circuit;

wherein a first signal is inputted to gates of the second transistor, the third transistor and the fourth transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

10. (Withdrawn) The semiconductor device according to claim 9, wherein the first transistor is an n-channel transistor, the second transistor is an n-channel transistor, the third transistor is an n-channel transistor, and the fourth transistor is a p-channel transistor.

11. (Withdrawn) A semiconductor device comprising:

a first transistor;

a second transistor;

a third transistor;

a fourth transistor;

a fifth transistor;

a sixth transistor;

a first power source applying a first potential;

a second power source applying a second potential;

a first circuit for generating a third potential which is different from the first potential and the second potential; and

a second circuit for generating a fourth potential which is different from the first potential and the second potential;

wherein one of a source and a drain of the first transistor and one of a source and a drain of the third transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor and one of a source and a drain of the fifth transistor is connected to the second power source;

wherein a gate of the second transistor is connected to the other of the source and the drain of the third transistor and to one of a source and a drain of the fourth transistor;

wherein the other of the source and the drain of the fourth transistor is connected to the first circuit;

wherein a gate of the first transistor is connected to the other of the source and the drain of the fifth transistor and to one of a source and a drain of the sixth transistor;

wherein the other of the source and the drain of the sixth transistor is connected to the second circuit;

wherein a first signal is inputted to gates of the third transistor, the fourth transistor, the fifth transistor, and the sixth transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

12. (Withdrawn) The semiconductor device according to claim 11, wherein the first transistor is an n-channel transistor, the second transistor is a p-channel transistor, the third transistor is a p-channel transistor, the fourth transistor is an n-channel

transistor, the fifth transistor is an n-channel transistor, and the sixth transistor is a p-channel transistor.

13. (Withdrawn) A semiconductor device comprising:

a first transistor;

a second transistor;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit including one third transistor or multiple third transistors connected in series;

wherein one of a source and a drain of the first transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to one terminal of the circuit;

wherein the other terminal of the circuit is connected to the second power source;

wherein a gate of the third transistor is connected to a drain thereof;

wherein a first signal is inputted to gates of the first transistor and the second transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

14. (Withdrawn) The semiconductor device according to claim 13, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is an n-channel transistor.

15. (Withdrawn) A semiconductor device comprising:

a first transistor;

a second transistor;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit including one third transistor or multiple third transistors connected in series;

wherein one terminal of the circuit is connected to the first power source;

wherein the other terminal of the circuit is connected to one of a source and a drain of the first transistor;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to the second power source;

wherein a gate of the third transistor is connected to a drain thereof;

wherein a first signal is inputted to gates of the first transistor and the second transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

16. (Withdrawn) The semiconductor device according to claim 15, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is a p-channel transistor.

17. (Withdrawn) A semiconductor device comprising:

a first transistor;

a second transistor;

a first power source applying a first potential;

a second power source applying a second potential;

a first circuit including one third transistor or multiple third transistors connected in series; and

a second circuit including one fourth transistor or multiple fourth transistors connected in series;

wherein one terminal of the second circuit is connected to the first power source;

wherein the other terminal of the second circuit is connected to one of a source and a drain of the first transistor;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to one terminal of the first circuit;

wherein the other terminal of the first circuit is connected to the second power source;

wherein a gate of the third transistor is connected to a drain thereof;

wherein a gate of the fourth transistor is connected to a drain thereof;

wherein a first signal is inputted to gates of the first transistor and the second transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

18. (Withdrawn) The semiconductor device according to claim 17, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, the third transistor is an n-channel transistor, and the fourth transistor is a p-channel transistor.

19.-21. (Canceled)

22. (Currently Amended) A semiconductor device comprising:

a first transistor;

a second transistor;

a plurality of inverters;

a first power source applying a first potential;

a second power source applying a second potential;

a first circuit for generating a third potential which is different from the first potential and the second potential; and

a second circuit for generating a fourth potential which is different from the first potential and the second potential,

wherein each of the plurality of inverters comprising:

a third transistor; and

a fourth transistor,

wherein one of a source and a drain of the second transistor is connected to the second power source,

wherein the other of the source and the drain of the second transistor is connected to each of the plurality of inverters,

wherein one of a source and a drain of the first transistor is connected to the first power source,

wherein the other of the source and the drain of the first transistor is connected to each of the plurality of inverters,

wherein a gate of the first transistor is connected to the second circuit,

wherein a gate of the second transistor is connected to the first circuit,

wherein a first signal is inputted to gates of the third transistor and the fourth transistor of each of the plurality of the inverters, and

wherein a second signal is outputted from ~~the other~~ one of [[the]] a source and [[the]] a drain of the third transistor and [[the]] one of [[the]] a source and [[the]] a drain of the fourth transistor of each of the plurality of the inverters.

23. (Previously Presented) The semiconductor device according to claim 22,

wherein the first circuit includes multiple resistors connected in series,

wherein an end of the multiple resistors is connected to the first power source,

wherein an end of another one of the multiple resistors is connected to the second power source, and

wherein the third potential is outputted from a connecting node of two resistors that are selected from the multiple resistors.

24. (Previously Presented) The semiconductor device according to claim 22,

wherein the second circuit includes multiple resistors connected in series,

wherein an end of the multiple resistors is connected to the first power source,

wherein an end of another one of the multiple resistors is connected to the second power source, and

wherein the fourth potential is outputted from a connecting node of two resistors that are selected from the multiple resistors.

25. (Currently Amended) An electronic appliance using the semiconductor device according to any one of claims 1, [[3, 5]] 3 and 22.

26. (Previously Presented) The semiconductor device according to claim 1,

wherein each of the multiple resistors has a resistance which is constant regardless a voltage applied thereto.

27. (Previously Presented) The semiconductor device according to claim 3,

wherein each of the multiple resistors has a resistance which is constant regardless a voltage applied thereto.

28. (Canceled)